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APPLICATION NOTE

ONE TECHNOLOGY WAY • P.O. BOX 9106 • NORWOOD, MASSACHUSETTS 02062-9106 • 617/329-4700

The Alexander Current-Feedback Audio Power Amplifier*

by Mark Alexander

This application note was written by Mark Alexander, who received his BSEE from the University of Toronto in 1981. As a consultant to Analog Devices, Mark describes a unique power amplifier topology that is the result of his long standing interest in audio power amplifier design and critical listening of audio systems.

The current-feedback approach presented here meets the traditional audio requirements of power amplifiers, but also adds the additional benefit of very high speed and bandwidth (200 V/μs slew rate, 1 MHz bandwidth) that results in excellent dynamic performance, and hence, sound quality.

INTRODUCTION

The subject of power amplifier design is one of those controversial areas of audio engineering that continues to receive intense debate, despite the fact that there are literally dozens of papers available to guide the designer. Many different topologies have evolved from the relatively modest beginnings of solid state power amplifier design in the late 1950s and early 1960s, and this has lead to a few very unique and original designs. A substantial number of transistorized amplifiers that were built during these early years were little more than redesigns of vacuum tube circuits with lower voltage supply rails, and often had performance levels that left a great deal to be desired. Quite a few of them sounded significantly worse than their thermionic predecessors. The "real revolution" in audio power amplifier design actually occurred during the 1970s and introduced such new innovations as direct coupling, fully complementary design, pseudo Class A biasing, and current dumping; not to mention the discovery of the importance of dynamic intermodulation distortion testing and its relationship to slew rate. Unfortunately, the plethora of so called "new" amplifier designs that have proliferated since this period are often variations of older circuits that originated during the 1970s, and generally feature only slight modifications to the input, output or gain stages.

Some designers have demonstrated rail-commutated output stages, which allow them to improve the operating efficiency of a big amplifier to such an extent that the huge amount of output transistor heat sinking usually necessary is reduced to that of a much lower power design. These can suffer from "switch over" distortion caused by the output stage switching between different supply rails, and can be quite objectionable. Certainly, high output power should not be obtained at the expense of inferior operating specifications, but this is indeed the case with certain types of amplifiers. Some clever design techniques do achieve quite impressive performance, however, albeit at the expense of greatly increased circuit complexity. Still other amplifiers dispense completely with the familiar principles of negative feedback, and their creators claim that their circuitry provides a sound more "open and lifelike," even though the distortion performance is usually poor. On the whole, though, most audio power amplifiers are essentially discrete copies of monolithic voltage feedback op amps, such as the 4136, but are invariably simplified to reduce the transistor count.

The purpose of this technical note is to introduce the audio designer to a truly new power amplifier topology, not an adaptation of an existing design, that offers exceptional performance on a par with the best of the available solid state designs (voltage feedback or otherwise). This new topology completely dispenses with the principles of global voltage feedback, so commonly used in most amplifiers, in favor of a design based instead on the principles of current feedback. In addition, this note addresses many of the important practical aspects of successfully getting a design off the ground, aside from choosing the basic core amplifier design. In almost all cases, having a good basic amplifier topology is not enough to guarantee that the final piece of equipment will perform to the original design expectations. Consequently, additional topics such as board layout,

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component selection, paralleling output devices, placement of high current wiring, and thermal design are considered as well.

A LITTLE BACKGROUND ON FEEDBACK

Before dissecting the new audio amplifier circuit in detail, some background on the differences in operational characteristics between voltage feedback and current feedback amplifiers is appropriate. Since it is likely that the reader may not have been previously exposed to the latter, an overview of voltage feedback followed by a look at the advantages of current feedback is necessary. This discussion will allow one to understand why circuits that make use of this relatively new topology are so important. Because the bandwidth of an audio amplifier is usually one of the most important specifications, a relatively simple equation for the upper −3 dB point is essential. Simplifying the current feedback amplifier and its attendant feedback network into a representative circuit model for nodal analysis provides the key to arriving at a compact, but reasonably accurate, expression for the frequency response. Appendix A has complete details of the circuit analysis.

The theoretical analysis of a voltage feedback circuit that often accompanies its frequent criticism has been well described in other works,[1] and thus will not be reiterated here. Since the original impetus behind the development of this new power amplifier design was a general dissatisfaction with the performance achievable by voltage feedback circuits, some discussion of their disadvantages is worthwhile. This will serve to set the stage for the in-depth discussion of current feedback amplifier analysis, in Appendix A. Although the analysis section can be skipped without disrupting the continuity of this note, the reader is encouraged to review it.

Constant gain bandwidth characteristics, resulting from the application of voltage feedback, present a problem if one requires reasonably high gain while simultaneously achieving wide closed-loop bandwidth. Some very high voltage power amplifiers may require gains as high as 50, for example, plus a bandwidth of several hundred kilohertz which obviously means that a gain bandwidth product in the range of 10 MHz to 20 MHz is needed. This is not easy to achieve, especially in a high voltage design. An additional problem with voltage feedback amplifiers is that their slew rate is usually limited by the transconductance stage which has a finite maximum output current, normally equal to the tail current of the differential input transistor pair, available to charge the compensation capacitor. High slew rate is very desirable in a large-signal audio power amplifier and mandates the use of large input-stage tail currents and small compensation capacitor values. Unfortunately, in the interests of amplifier stability, reducing the value of the compensation capacitor requires some degeneration of the input stage (to reduce its transconductance) which thus reduces the open-loop gain. This action reduces the loop gain available in the audio band and causes an increase in THD products, since it is the loop gain that serves to reduce the open-loop amplifier distortion, most of which originates in the highly nonlinear output stage. What all this boils down to is the fact that a difficult trade-off has to be made between stability, open-loop gain, and slew rate without compromising the overall ac performance and transient response. Clearly, a global voltage feedback scheme may not necessarily be the optimum choice for ultrahigh performance audio power amplifiers, and in some cases it will not even be possible to meet all the design goals using this topology.

Current feedback operational amplifiers were originally introduced because they overcame the bandwidth variation, inversely proportional to closed-loop gain, exhibited by voltage feedback amplifiers. They still show a slight variation of bandwidth, however, as the gain is increased above unity, but it is much less significant than with the latter. In fact, current feedback amplifiers don't begin to behave like voltage feedback amplifiers until the closed-loop gain is made quite large (~50). The simplified model of a current feedback amplifier in Figure 1 shows that it uses a unity gain input buffer whose output current is fed, via a bidirectional current mirror, into a transimpedance gain stage. The voltage generated here is then buffered and fed to the output terminal. Typical values for R_T are quite high, usually several hundred kilohms or even a few megohms. R_{INV} is the output resistance of the input buffer, and feedback resistors R_1 and R_2 set the input-to-output voltage gain in a fashion somewhat similar to that of a conventional op amp. Here, however, it is an error current I_1 that sustains the output voltage and not an error voltage.

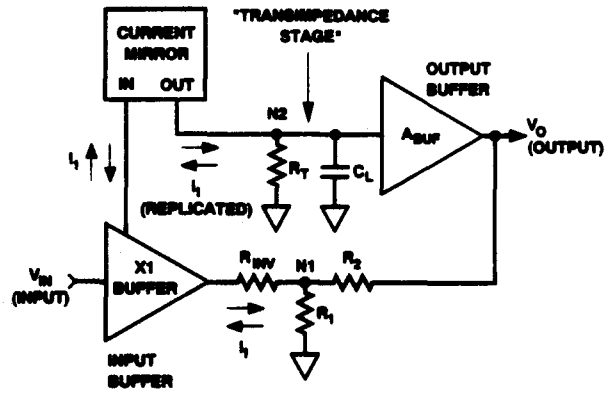


Figure 1. The Model of a Current Feedback Amplifier Shows that an Error Current, I_1, Determines the Overall Output Voltage.

The concept of a finite gain bandwidth product can also be applied to a current feedback amplifier as a measure of its performance, although it is only meaningful at high gains. Arguably, the most important attribute of this topology is that the amount of current available to charge the compensation capacitor during output slewing is proportional to the difference between the actual and final output voltages, just like a simple RC circuit. As such, there is theoretically no slew rate limit with this topology, which makes it very attractive for an audio power amplifier. Practical circuit limitations inevitably

impose a restriction on the maximum current level that can be handled in the gain stage of a current feedback amplifier, however, and it is this limiting that gives rise to a finite slew rate. Still, the slew rates achievable with these types of circuits are often higher by as much as a factor of 5 (or greater) than their voltage feedback counterparts, for a given quiescent supply current. Current feedback represents a much more logical choice for a power amplifier than voltage feedback, and this will be demonstrated.

POWER AMPLIFIER CIRCUIT TOPOLOGY

Prior to looking at the actual amplifier circuit, the simplified block diagram of Figure 2 will be considered to help understand how the overall design works on a system level. This will make the final amplifier circuit easier to follow. As may be gathered from Figure 2, this is a rather unconventional design, in which there are two op amp input stages feeding a single gain stage and power output buffer. By considering this design one block at a time, however, it is becomes easier to grasp the way in which each of the major sections interacts with one another.

The Input Stage

The input buffer used in this power amplifier is simply a conventional voltage feedback op amp chosen for its excellent audio characteristics, and reasonably high output current capability. This ensures that the limiting factor in terms of overall amplifier performance will be the current feedback gain block and not the input stage. The output current from input amplifier A_1 is taken from its power supply pins and fed to the emitters of a pair of common base cascode transistors that provide regulated dc voltages for the op amps. At first glance this might appear to be a very strange connection, because the power supply pins of A_1 are used as outputs and its output is used as an input. However, this is in accordance with the model shown in Figure 1 since the output current from the input buffer must be fed, via the bidirectional current mirror, into the transimpedance gain stage. It is here that the high output voltage is ultimately generated, prior to buffering by the unity gain output stage. The half-wave rectification action of A_1's output current, due to its class AB output stage, causes the two current mirrors to receive complementary input currents. When A_1 is sourcing output current, it causes a corresponding increase in the current of the upper mirror and a decrease in that of the lower mirror. This forces the voltage at the output of the transimpedance stage to swing positive. For cases where A_1 is sinking current, exactly the opposite is true. A current mode gain stage arrangement such as this is fully complementary and truly push-pull, which means it should exhibit low even-order distortion. Note that the quiescent supply current of A_1 conveniently serves to bias the two current mirrors that sit referenced to each power supply rail, thus providing an appropriate operating point for the transimpedance stage and bias voltage generator.

In most commercially available current feedback amplifiers, the input buffer stage has a gain of unity and is generally of an open-loop design. Here, an op amp is being used as the input stage instead and thus can be configured to provide some gain. This is extremely easy to do since it only involves tapping the shunt resistor to ground at the output of A_1. The overall amplifier midband gain is therefore:

$$A_V = \left(1 + \frac{R_7}{R_6}\right)\left(1 + \frac{R_8}{R_6 + R_7}\right) \qquad (1)$$

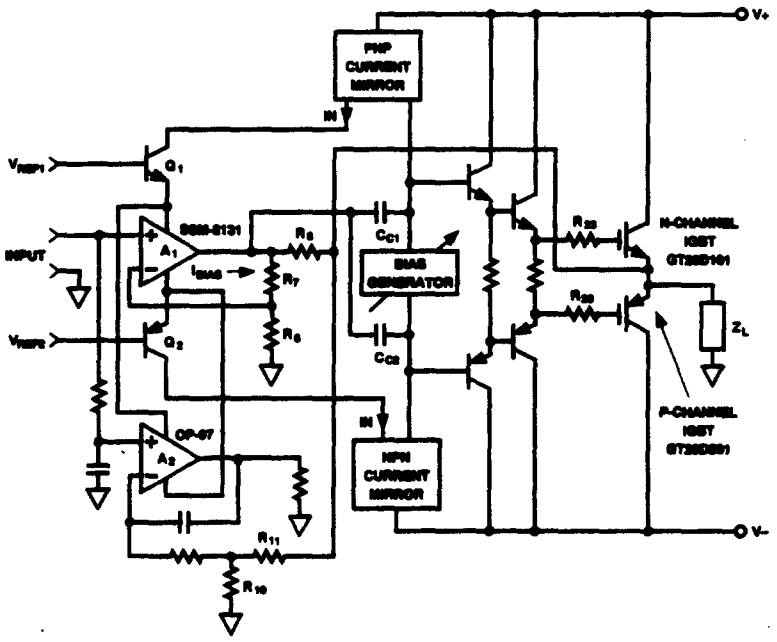


Figure 2. A Simplified Block Diagram of the Amplifier Shows that the Input Amplifiers, A_1 and A_2, Feed a Common Gain Stage and Output Buffer.

The Gain Stage and Frequency Compensation

The outputs of the two current mirrors that are connected to each supply rail feed an adjustable voltage bias generator which provides the necessary bias for class AB operation of the complementary MOS-IGBT (Metal-Oxide-Semiconductor Insulated-Gate-Bipolar-Transistor) output stage. The bias generator is designed to have very low output impedance over the operating frequency range of the amplifier. Compensation is provided by C_{C1} and C_{C2}; two capacitors are used instead of one to keep the structure of the gain stage symmetrical. Unlike the simplified current feedback model shown in Figure 1, this design has the compensation capacitors returned to the feedback summing node instead of ground. This alternate connection has a very beneficial effect on the amplifier step response when it is loaded by a fairly low value impedance such as a loudspeaker.

An IGBT emitter follower output stage, such as the one used in this amplifier, has a transfer function that contains two poles and a real zero plus the usual dc gain term of slightly less than unity. When the amplifier drives high values of load impedance, such as the feedback resistors alone, the two output stage poles are quite high in frequency (usually above 20 MHz), and contribute little excess phase shift within the amplifier's passband. Quite a different situation arises when a load is connected to the output of the amplifier. The two poles in the output stage now split apart, and the dominant one becomes sufficiently low in frequency that it contributes excess phase shift at lower frequencies within the amplifiers' passband. This can cause a considerable problem if the compensation scheme in Figure 1 is used since it may result in undesirable ringing on the edges of a square wave. The compensation scheme of Figure 2 overcomes this problem by inserting a high frequency closed-loop zero that tends to make the amplifier more stable. Also, this compensation arrangement allows the use of smaller capacitors than with the original scheme. Appendix A shows the complete response of the amplifier when this alternate compensation scheme is used. If we assume that the small signal transresistance, R_T, is quite high and also that the output buffer gain is near unity, then the closed-loop pole and zero will occur at frequencies given by:

$$f_{POLE} \cong \frac{1}{2\pi\left(2R_8 + \frac{R_8}{R_6 + R_7} R_{INV}\right) C_{C12}} \quad (2)$$

and

$$f_{ZERO} = \frac{\left(1 + \frac{R_8}{R_6 + R_7}\right)}{4\pi R_8 C_{C12}} \quad (3)$$

where C_{C12} is the sum of C_{C1} and C_{C2}. Notice that the frequency at which the zero occurs is approximately equal to the closed-loop bandwidth multiplied by the gain of the current feedback loop, if R_{INV} is fairly small in value. These equations, plus Equation (1), are the necessary design formulas needed to determine the gain and small signal bandwidth of this amplifier. Later on it will be demonstrated that the mathematical theory and actual measurements made on the circuit do indeed correlate very well with each other.

Driver and Output Stages

This part of the power amplifier design is quite conventional, relatively speaking, and no attempt was made to use error correction or pseudo class A biasing schemes to lower the output stage crossover distortion. Since the primary design objective for this amplifier was wide bandwidth and high slew rate, it was felt that any additional circuitry following the transimpedance gain stage might degrade the closed-loop stability. Besides, low crossover distortion can be achieved by running the output transistors at a sufficiently (but not excessively) high idling current. A simple double emitter follower driver stage, therefore, was chosen to buffer the voltage generated by the gain stage and feed it to the gates of the power IGBTs. This driver stage is capable of providing several hundred milliamps of charging current for the IGBT gate capacitances while the output is slewing, and is mandatory in a high speed design such as this.

DC Control Amplifier

The purpose of this additional input stage is to provide an accurate, low drift, dc gain path to the main output that is independent of the ac gain path and its poor dc characteristics. In the original version of this amplifier, expensive precision matched NPN and PNP dual transistors were used in the two current mirrors, but no dc control amplifier was used. It was incorrectly assumed that precise matching of the transistors in each mirror would result in very low output offset voltage, as long as the input buffer had reasonably low input offset voltage as well. As it happens, this is not the case with a current feedback amplifier. Any mismatch between the two current mirrors results in a finite amount of bias current appearing at the output terminal of the input buffer, which must flow through feedback resistor R_8 to the output. It cannot flow through R_6 and R_7 to ground, because the current in these resistors is set only by the voltage appearing at the output of the input buffer. The output offset voltage, without the dc control amplifier is thus:

$$V_{OOS} = V_{IOS\,(A1)}\left(1 + \frac{R_7}{R_6}\right)\left(1 + \frac{R_8}{R_6 + R_7}\right) + I_{BIAS} R_8 \quad (4)$$

Normally, V_{IOS} (A_1) can be made quite small by using a low offset op amp. Unfortunately, the output terminal bias current, I_{BIAS}, can be as large as 100 µA under static conditions and even larger if a thermal gradient exists between the two mirrors on the power amplifier driver board. This can easily lead to an output offset in excess of 100 mV, which changes as the amplifier warms up. A large offset like this is likely to cause an audible click when the relay that connects the loudspeakers to the amplifier is energized, and is generally undesirable.

The solution to these problems is a low frequency servo-loop that controls the dc output voltage, independently of any low frequency current or voltage fluctuations in

the main current feedback gain path. This is facilitated by the use of a second low power precision op amp, A_2, that is configured as an integrator with very low crossover frequency (less than 5 Hz). The low crossover frequency ensures that the integrator will not have any effect on the performance of the overall amplifier in the audio band. Voltage feedback is applied from the main output back to the input of the integrator through resistors R_{10} and R_{11}, which set the closed-loop dc gain. This gain is made equal to that given by equation (1). Since A_2 drives a resistor connected to ground, as shown in Figure 2, it behaves as an operational transconductance amplifier with the output current taken from its power supply terminals. This compensating output current is then fed to the two common-base regulator transistors where it is summed with the signal current from the power supply terminals of A_1. The output current of A_2 is thus forced to cancel I_{BIAS} almost exactly because the dc gain of the integrator, coupled with the additional gain produced by the transimpedance stage, is very high. Consequently, the integrating control loop completely overrides the current feedback loop at dc and the output offset is reduced from that given by Equation (4) to:

$$V_{OOS} = V_{IOS\,(A2)}\left(1 + \frac{R_{11}}{R_{10}}\right) \qquad (5)$$

This means that it can be made arbitrarily small through the choice of a low offset amplifier for A_2. Here the cost of an additional op amp is more than offset by not having to use expensive matched NPN and PNP dual transistors in the current mirrors.

AMPLIFIER CIRCUIT DESIGN

The complete circuit diagram for one channel of the amplifier is shown in Figure 3, and an accompanying parts list is included in Appendix B. This design utilizes 2 IC op amps, 17 bipolar transistors in the gain and driver stages, and at least 2 complementary IGBT power transistors from Toshiba in the output stage. These recently introduced devices are essentially similar to power MOSFETs in that they have a very high impedance input terminal (the gate) and square-law transfer characteristics, but are manufactured using a slightly modified double diffused MOS process. Unlike power MOSFETs, however, they feature consistently higher current handling capability for N- and P-channel transistors of a given die size. This allows one to get by with a smaller die size IGBT output stage than one using MOSFETs, thus providing a fairly substantial cost savings (especially on the P-channel transistors). The driver stage in this amplifier can easily accommodate multiple pairs of power devices in the output stage, because of its high peak current drive capability, but just a single pair of 250 V, 20 A IGBTs was used in the version that was characterized here. Power supply voltages for the driver board and output stage may range from ±20 V to ±75 V. Most of the components that mount on the compact driver board, the layout of which is shown in Figure 4, are quite readily available and inexpensive.

An input filter with a cutoff frequency of approximately 2 MHz precedes the input stage. It was included to reduce the potential for RF interference problems, and to eliminate the possibility of the amplifier oscillating on power-up with the input left floating (something that was noticed during the original development of this topology). The filter is formed by the 100 Ω input resistor and 750 pF shunt capacitor. A 100 kΩ resistor is connected to ground at the input of A_1, and provides the necessary dc bias current path to ground if the input is inadvertently left open. The overall amplifier gain is set by R_6, R_7, and R_8, and substituting the values of these resistors into equation (1) yields a figure of 24.087 or 27.64 dB. If more gain from the circuit is desired, the values of R_6 and R_7 should be changed, but their sum should be kept approximately equal to 50 Ω so that the gain of the current feedback section stays constant (at about a factor of 16). By simply swapping the 16.5 Ω and 33.2 Ω resistors, for example, the gain of the input stage becomes approximately equal to 3, and the gain of the overall amplifier increases to a factor of 48.47 or 33.7 dB. In fact, the gain of the input stage can be made as large as 20 dB before its bandwidth drops below that of the rest of the amplifier.

The references for the two common-base regulator transistors (Q_1 and Q_2), which provide stable supply voltages for the op amps, are actually two pairs of standard NPN bipolar transistors (2N3904s) used as Zener diodes (Q_{14} through Q_{17}). They are connected in series (with their collector leads clipped off) to obtain a net breakdown voltage of around 15 V for the pair . There really is a good reason for using such an arrangement since it would obviously be easier to use a 15 V "Zener" diode, as opposed to this seemingly more complicated approach. In reality, the connection of two bipolar transistors in this manner exhibits significantly less low frequency noise than the 15 V "avalanche" diodes, as they are more appropriately called, and is actually more cost effective. The composite Zeners are bypassed with 10 µF 25 V tantalum capacitors, used mainly for reasons of economy and size, which filter out residual noise from the diodes as well as the power supply rails. Two resistors marked R_{BIAS} on the circuit diagram (R_1 and R_2), which are connected to each supply, serve to bias Zener connected transistors Q_{14} through Q_{17} and should be chosen such that with nominal power supply operating voltages (anywhere from 50 to 70 volts) about 1 mA of current will flow through them.

The two Wilson current mirrors connected to each rail, and fed from the collectors of Q_1 and Q_2, are formed from a low voltage transistor, a diode and a high voltage transistor (2N5551 or 2N5401). They are degenerated somewhat with 100 Ω 1% resistors to improve matching. Anti-saturation diodes (D_2 through D_5) have been included to prevent storage time problems with the cascode transistors (Q_4 and Q_5) in either of the two mirrors during clipping, and this results in extremely rapid recovery from overdrive. It should be noted that the onset of clipping in the transimpedance stage will occur at

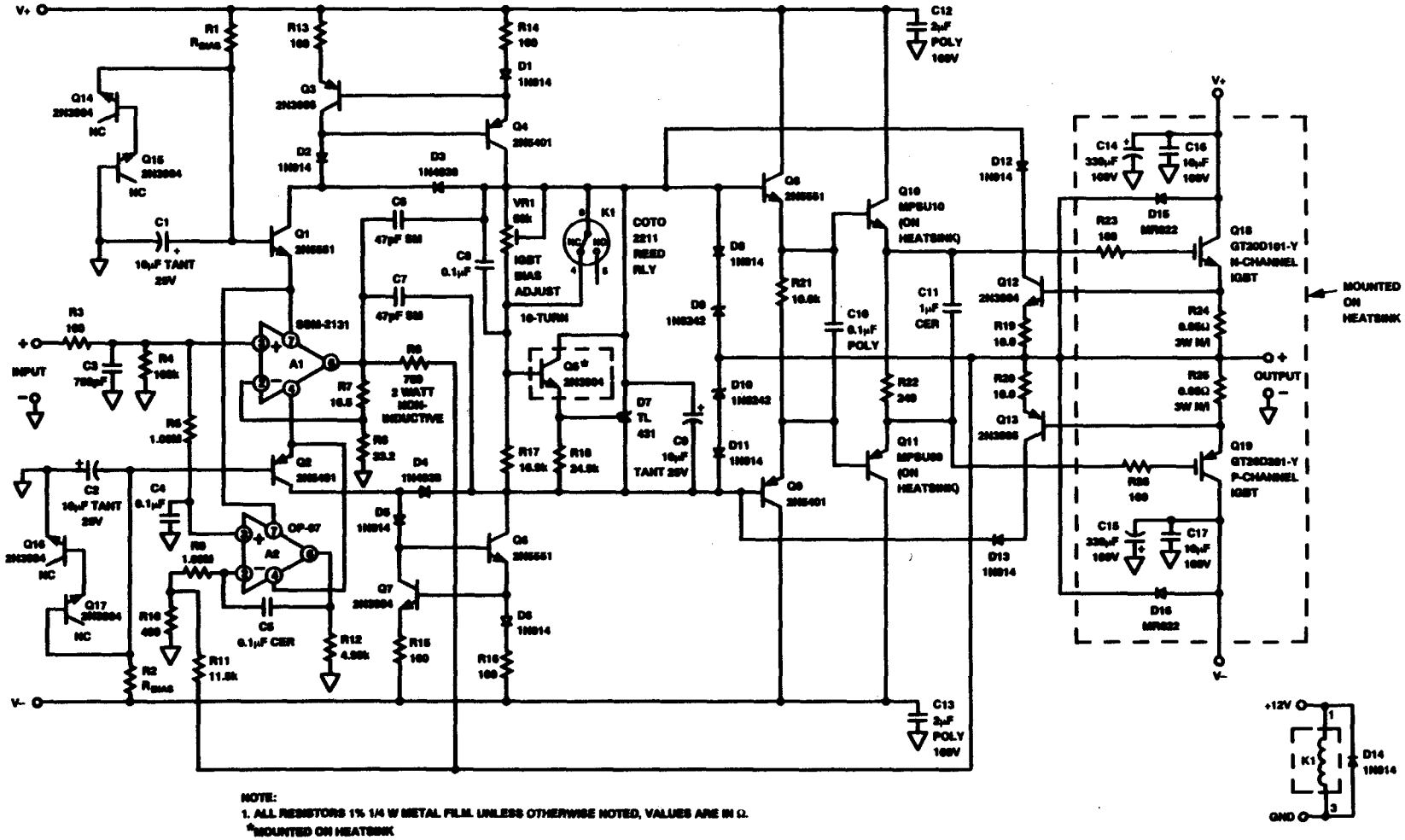


Figure 3. The Complete Amplifier Circuit Diagram Shows that Inexpensive Small-Signal Silicon Is Used Throughout to Minimize Overall Cost.

about 2 V from either power supply rail for very small overdrive conditions, but hard clipping in this stage will actually be dependent on the current limit of the input amplifier A_1. This occurs because, during hard clipping, the current summing network connected to the output of A_1 is no longer balanced and significant current can flow in its output stage. Consequently, the current in the mirrors increases very rapidly up to the value of A_1's maximum output capability (usually 30 mA to 40 mA), causing a corresponding voltage drop across the aforementioned 100 Ω resistors. The effect of this excessive current in the mirrors is such that it causes the clipped signal to "pull in" slightly from the rails, as the amplifier is driven harder and harder into its overload region. It is very important not to let the circuit stay in this condition for any significant period of time, since the power dissipation in Q_1 and Q_2 will increase far beyond their nominally rated value of a few hundred milliwatts. Peak dissipation in these transistors can reach as much as 1.5 W to 2 W, with typical rail voltages of 50 to 70 volts; therefore, very large dc input signals or low frequency square waves should be avoided. If these operating conditions are anticipated, however, clip-on heat sinks for Q_1 and Q_2 are mandatory.

Frequency compensation in this particular design is provided by two 47 pF compensation capacitors that are connected to the feedback summing node (C_6 and C_7), as mentioned previously. This results in a total value of 94 pF. The reason such a large value of capacitance was chosen is quite simple: it completely swamps out any nonlinear voltage dependent capacitances that are present at the high impedance gain node, resulting in constant amplifier bandwidth as the supply voltage is varied. Concerns about too low a slew rate, with such large compensation capacitors, are usually justified in a voltage feedback amplifiers, but here there is as much as 30 mA of current available to charge them and slew rate limiting will not normally be encountered.

A calculation of the expected frequency response of the amplifier is now in order, and can be accomplished quite easily by substituting the value of 94 pF for C_{C12}, and the values of 750 Ω for R_8, 16.5 Ω for R_7, and 33.2 Ω for R_6 into Equation (2). The value for R_{INV} is a little more difficult to determine since we must know *a priori* what the value of the closed-loop output resistance of A_1 is, at the overall −3 dB point of the amplifier. The solution to this problem actually involves a little bit of circular reasoning, but the motive behind it is rather easy to see. If Equation (2) is evaluated initially without considering the effect of R_{INV}, a closed-loop bandwidth of 1.12 MHz is calculated. Since the effect of a finite R_{INV} is to lower the bandwidth somewhat, a prediction of the final amplifier closed-loop bandwidth will allow an initial guess for this parameter to be made. In this case a prediction of a final closed-loop bandwidth of 1 MHz is made. If we now take the open-loop output resistance of A_1 from its data sheet (about 70 Ω) and divide it by one plus the value of its loop gain at the predicted −3 dB point of 1 MHz (about 7.68), a value of 9.11 Ω is obtained. When this estimate for R_{INV} is included in Equation (2), an overall closed-loop bandwidth of 1.034 MHz is the final result. This is really very close to the original guess of 1 MHz, and it seems that no further iteration will be necessary to get closer to an acceptable answer. It should now be plainly apparent that extraordinarily wide closed-loop bandwidth seems rather easy to come by in a current feedback power amplifier, even when the compensation capacitors are quite large. For this reason, careful board layout and wiring techniques are of tantamount importance in actually getting a design such as this to work properly without oscillating.

The output stage bias voltage generator, connected between the collectors of Q_4 and Q_6, is formed from a programmable shunt regulator (D_7), with an NPN emitter-follower buffer (Q_5) driving its control input. This buffer is not normally required in most applications because the control input bias current of D_7 (a TL431) is only a few microamps, but it is included here for thermal compensation of the output stage idling current. A common problem with biasing output stages that use vertical DMOS devices (MOSFETs and IGBTs) is that at moderately low current levels, the decrease in V_{TH} of approximately 3 mV/°C causes the collector current to increase for a fixed gate-to-emitter bias voltage. If transistor Q_5 is securely mounted on the same heat sink as the power IGBT output stage, its V_{BE} will decrease as the output transistors heat up. This decrease in V_{BE} of about 2 mV/°C, which is multiplied up in the bias generator by approximately a factor of three, thus helps to stabilize the quiescent current in the IGBT output stage. A form-C relay can also be included across the 50 kΩ bias adjustment pot (VR_1), as shown, to allow the amplifier to be powered up with zero bias voltage on the output transistors. This feature, when used in conjunction with resistive surge protection schemes for the main filter capacitors (and bridge rectifiers) during power up, will prevent any static voltage drop across the current limiting resistor due to the amplifier class AB idling current.

Some means must be provided, as well, to protect the output transistors from any condition that could cause their gate-to-emitter voltages to exceed the maximum allowed value of ±20 V. Thus, Zener diodes D_9 and D_{10} are connected from either side of the bias generator to the main output, and prevent the voltage seen between the gain stage and the emitters of the IGBTs from exceeding more than about 12 V.

The IGBT output stage is operated in a complementary emitter-follower configuration running at an idling current of about 100 mA, and series gate resistors R_{23} and R_{26} are included to limit the frequency response. This mitigates any tendency, in the fairly wideband output stage, towards parasitic oscillation. Current in the output stage is sensed across two low value resistors, R_{24} and R_{25}, connected in series with the emitters of the IGBTs. As the voltage drop across either of these two resistors increases towards 0.7 V, Q_{12} or Q_{13} will begin to conduct current away from the gain stage and thus limit the

output voltage. This is a convenient way to limit the current in the output stage to a safe value. Emitter degeneration resistors (10 Ω) must be used in conjunction with the two limiter transistors, Q_{12} and Q_{13}, because this circuit has quite a bit of gain when active and tends to oscillate slightly at high frequencies. Since these transistors must sink or source all the current from the transimpedance stage (up to the current limit of A_1) when the output current is being limited, the voltage across the 10 Ω resistors will increase slightly as the amplifier is driven into hard limiting. This causes a corresponding increase in the actual value of limited current, resulting in a somewhat "soft" limiting curve.

Of course, current limiting alone is not enough to guarantee power transistor integrity if short circuits to ground at the output are anticipated. This results from the fact that excessive power dissipation in the output stage will still occur if the current limit is set fairly high (actually a very desirable attribute in a modern amplifier). Fusing the power supply feed to the output stage will usually be necessary for protection of the power transistors.

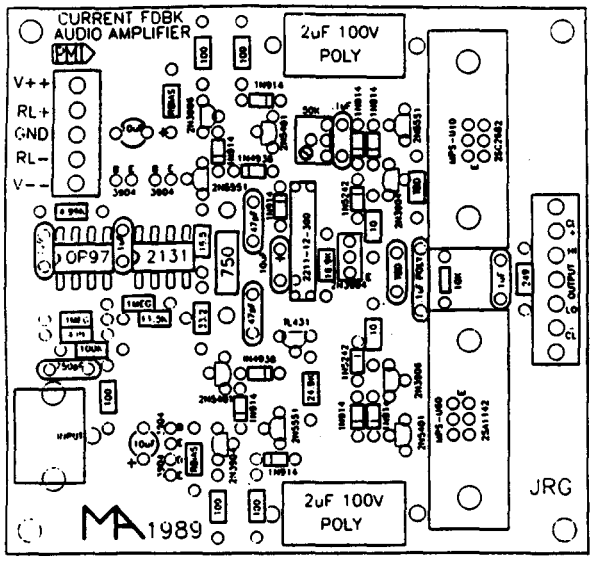
PRACTICAL CIRCUIT CONSIDERATIONS

It is often mistakenly assumed that once a respectable topology has been chosen for a power amplifier, it is a simple task to construct a completed unit that meets all the original design goals. In fact, getting the physical details of an amplifier's construction properly sorted out can be just as time consuming as the actual design of the driver electronics themselves.

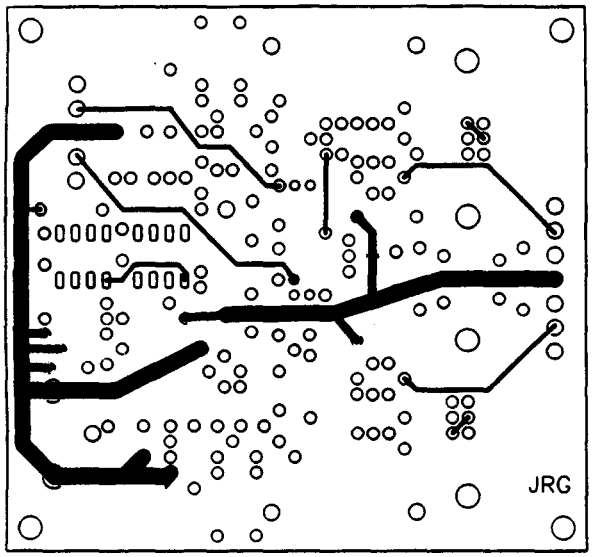
Circuit Board Layout

This is probably one of the most critical elements for a wide bandwidth audio power amplifier. The key to good board layout for this design is to keep trace lengths to an absolute minimum wherever possible, and to keep the overall layout very small in physical size. Figure 4 shows the layout of the board used to characterize this new topology, and as can be seen, the component packing density is reasonably high—it measures less than 9 cm on a side. The layout of the driver board actually follows the amplifier circuit diagram fairly closely in orientation, since it was begun on the left hand side where the input stage resides, and finished on the right where the output stage drivers are located.

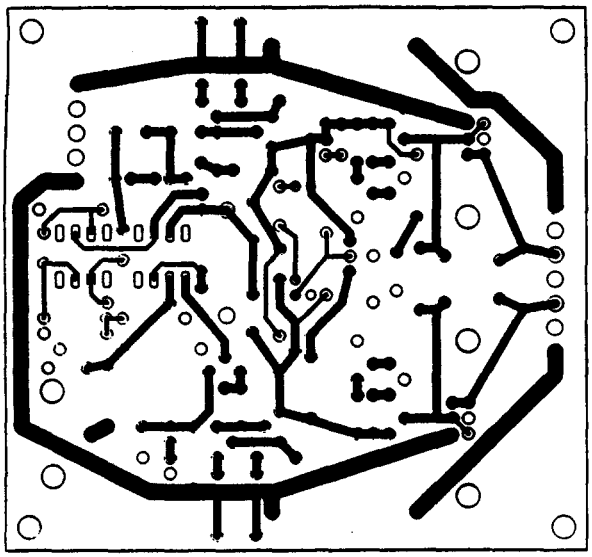
Power supply busses travel along the top and bottom edges of the board, thus providing a convenient means of picking off power for the various stages. The two polyfilm bypass capacitors on the board actually have their own ground return paths that are independently isolated from the signal ground bus near the input stage. This may seem a like a subtle refinement, but on the original layout the bypass capacitors shared the same ground bus as the input stage, and strange low level oscillations were noticed on the first prototypes. It turned out that the oscillation was occurring as a result of the discharging of the bypass capacitors into the driver transistors (and ultimately the gates of the output



a. Topside Silkscreening



b. Topside Layout



c. Bottomside Layout

Figure 4. A Compact Driver Board Contains All Amplifier Circuitry Except the IGBT Output Stage.

transistors) due to an initial perturbation in the circuit. This initial disturbance eventually lead to a self sustaining relaxation oscillation (of a few hundred hertz) because the ground bus surge, as the capacitors were discharging, was sufficiently large so as to be coupled back into the input stage of the amplifier. The improved layout of Figure 4 does not exhibit this anomaly.

Critical Component Selection

Some of the resistors in this design require great care in their selection, since the wrong type of resistive element will lead to unexpectedly poor performance. In particular, the 750 Ω feedback resistor R_8 should be an oversized completely noninductive metal film power resistor with a dissipation rating of at least 2 W (remember that the peak current in this component may be as high as 75 mA). Failure to use a resistor with a high enough power rating will very likely lead to thermal modulation of the actual resistance value and a corresponding increase in overall amplifier intermodulation distortion when large low frequency input signal components are present. Additionally, a low temperature coefficient of resistance is very desirable for this part. The current sensing resistors in the output stage (R_{24} and R_{25}) should also be of the low or noninductive variety. Since the short rise time of the amplifier (approximately 350 ns) means that a large di/dt in the load, and hence these resistors, can occur, any excessive inductance will cause the voltage across them to increase during fast edge transitions thus causing premature current limiting.

Input amplifier A_1 plays a significant role in the overall performance of the amplifier. It must possess all the desirable characteristics of a good line level audio op amp (namely low distortion, high slew rate and wide gain bandwidth product), plus it must have good output current capability as well. The SSM2131 BiFET audio op amp with a GBW of 10 MHz and slew rate of 40 V/μs more than meets the requirements for this design. Also, amplifier A_2 in the integrating dc control stage must have very low input offset current in addition to low offset voltage. This is because 1 MΩ resistors are used, in series with its input pins, to obtain the long time constant needed in this stage. Too large an input offset current would cause a sufficiently large differential dc error to appear across these resistors (many mV) and it would render a low input offset voltage op amp totally useless. The OP-97 adequately satisfies these requirements with an input offset current of only 30 pA and offset voltage of 30 μV.

Paralleling Output Transistors

This is an extremely important topic because most amplifiers will use more than one pair of output transistors per channel, so that low impedance loads can be accommodated without the output stage self-destructing. Since the maximum power dissipation in the output stage increases with decreasing load impedance, it is desirable to ensure adequate static and dynamic current sharing amongst all the output transistors. This will minimize the junction-to-case temperature rise in any one output device. Power MOSFET output stages can be effectively made to share current by means of tight thermal coupling between all transistors, and through the inclusion of appropriately valued series source-ballasting resistors. There is no reason to believe that power IGBT output stages, with their very similar square law transfer characteristics, will behave any differently if the same techniques are employed.

Typically for best current sharing in a MOSFET output stage, the value of the source resistors should be >>1/gm of each transistor over its desired drain current range. Since the transconductance is lowest at the output stage quiescent point, using this value of gm should guarantee sharing over the full output current range. Unfortunately, in practice this may lead to rather large resistance values and correspondingly large voltage drops when high values of load current are being delivered. A better solution is to do a limited amount of prescreening on the N- and P-channel IGBTs to eliminate any devices with larger than average characteristic deviations in V_{TH} and gm (at the idling point). Once this is done, it becomes feasible to use series emitter resistors in the range of 0.2/gm to 0.5/gm, which will help to minimize the voltage drop. For the Toshiba IGBT output devices used in this design, the typical gm at an emitter current of around 100 mA is close to 1S. For example, if an eight transistor output stage is needed that must have a total idling current of 400 mA, series emitter resistors in the range of 0.2 Ω to 0.5 Ω are acceptable along with some limited screening of the output transistors prior to installation.

Wiring Techniques

Some amplifier designers relegate power supply and output terminal wiring to the lowest level of the design phase. However, since these wires may carry large pulsating currents with a harmonic content well above the audio band, it pays to devote some attention to this task. Wiring is probably one of the most critical things that must be accomplished successfully, if the final design is to get anywhere close to the performance measured on a prototype breadboard (where the wires are normally quite short). Usually the layout of the power supply wiring is not particularly well controlled, but some very simple rules should be observed that will maximize the likelihood of success at first power up.

One of the most important rules in wiring layout is to use twisted pairs for the forward and return currents paths in any loop. This minimizes the series inductance of the conductors, since inductance increases with cross sectional loop area. Thus all power supply wires from the filter capacitors to the amplifier output stage(s) (and driver boards) should be twisted together, as shown in the system connection diagram of Figure 5. Fuses are placed in series with the power rails to protect the output stage in the event that an accidental short circuit in the load occurs. They should be of the fast blow type, and must be rated appropriately so that they will not

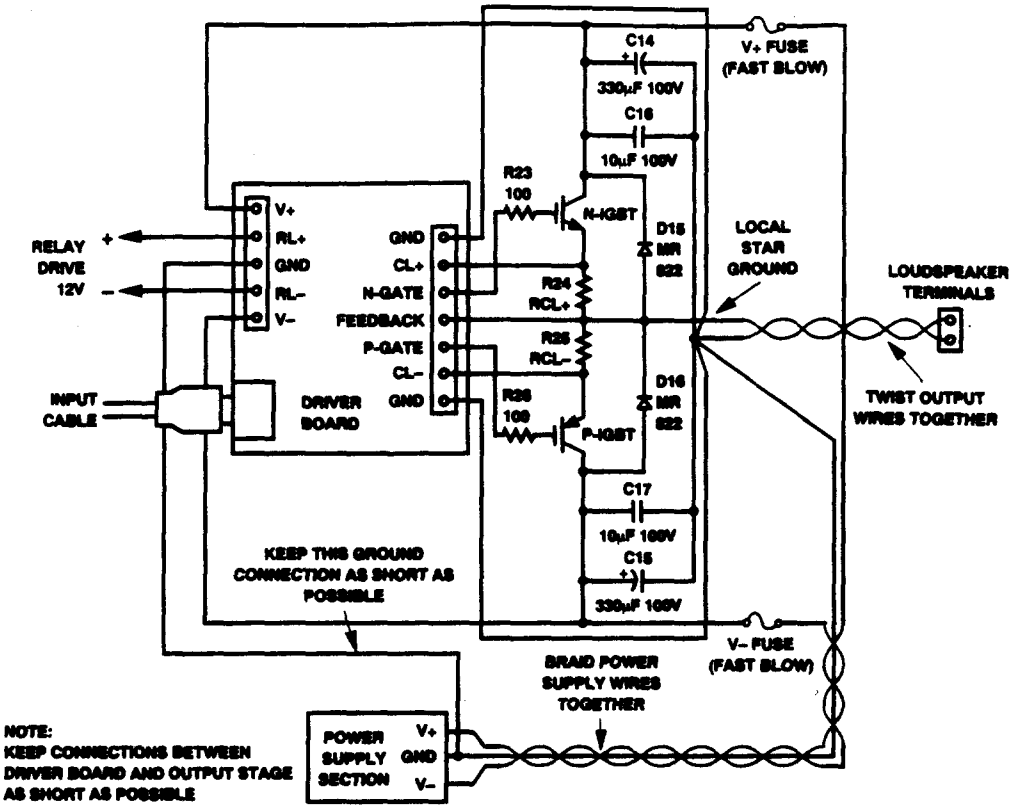


Figure 5. A Power Wiring Scheme Requires Proper Attention to Detail If Low Distortion Is to Be Achieved.

open up under peak output power levels. The wires that run from the output stage to the loudspeaker connectors should also be twisted together, as shown, to minimize their inductance. All interconnections between the driver boards and their respective output stages should be kept very short, in the interests of closed-loop stability. The series gate resistors for the IGBTs should be connected directly at the package terminals of these devices.

These tips are all a definite step in the right direction, but there is something else to consider that is decidedly not obvious. Since the positive and negative supply leads which feed the output stage(s) have half-wave rectified current waveforms, as shown in Figure 6, the harmonic current (occurring at even multiples of the fundamental output frequency) circulates in the loop formed between the power supply capacitors and the output transistors[2]. If there is any mutual inductance between these power supply leads and the output terminal loop, after the point at which negative feedback has been extracted, even order distortion components can be induced in the output that cannot be attenuated by the feedback action of the amplifier. For a typical amplifier with $R_L = 8\ \Omega$ and sinusoidal excitation, then at an output frequency f = 10 kHz, the induced second harmonic component in the output loop will be approximately 0.33% per µH of mutual inductance. It should be noted that the magnitude of the induced distortion components is proportional to the output frequency (i.e., they get larger as the frequency goes up), which can be minimized by keeping the power input and speaker wiring runs perpendicular to each other. Thus the output transistors should be physically connected to the power supply feed and output terminal cabling as shown in Figure 7. This approach minimizes the mutual coupling between the power input and output paths of the amplifier.

Heatsinking and Thermal Considerations

Heatsink selection should never be underestimated because it is one of those critical areas that, if neglected, will inevitably result in damage to the output transistors from excessive junction temperature. In most class AB power amplifiers, the total dissipation in the output stage is split equally between the two banks of output transistors (the N-channel units and the P-channel units). An equation that relates the power supply rail voltage and load impedance to the total maximum output stage power dissipation, under sinusoidal excitation, is given by:

$$P_{Diss}\,(max) = \frac{2\,V_{CC}^2}{\pi^2 |Z_L| \cos\theta} \qquad (6)$$

where θ is the phase angle of the load. As an example, consider the case of an amplifier with a two transistor output stage powered by ±60 V rails, and loaded by an impedance of 8 Ω with a phase angle of +30°. Under these conditions the maximum dissipated power will be 105.3 W. The Toshiba N- and P-channel IGBTs are rated for 180 W dissipation at a T_C of 25°C, but this is derated to zero at a T_C of 150°C. The junction-to-case thermal resistance ($R_{\theta JC}$) for these transistors is calculated by dividing the total difference in case temperature change (125°C) by that of the total change in power dissipation

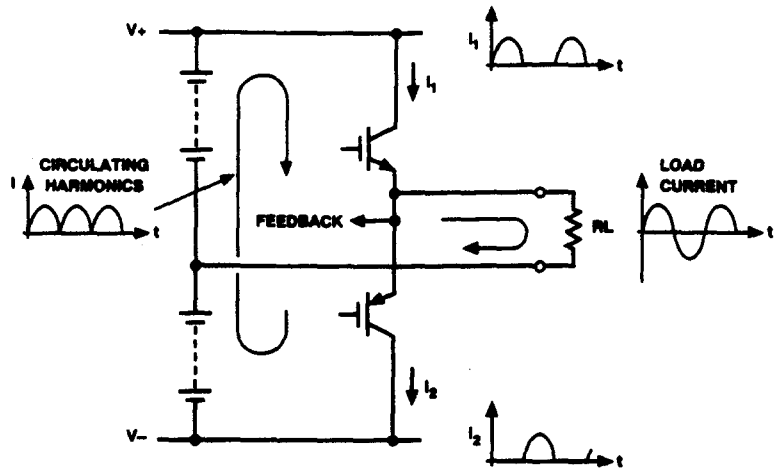


Figure 6. Harmonic Currents in a Power Amplifier Circulate Between the Supplies and the Class AB Output Stage.

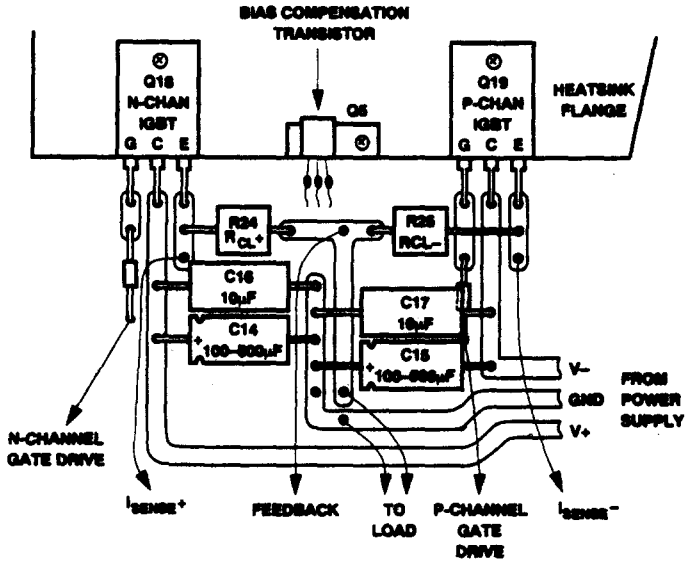


Figure 7. The Preferred Output Stage Layout and Component Placement

(180 W). This results in a figure of 0.694°C/W. Since the total power dissipated in the output stage is split equally between the two transistors, the effective $R_{\theta JC}$ is equal to 0.694/2 or 0.347°C/W. To ensure that the output stage transistors do not reach their maximum allowed junction temperature of 150°C, the total thermal resistance from junction-to-ambient (assuming T_A = 25°C) must not be greater than 125°C/105.3 W or 1.19°C/W. When the junction-to-case thermal resistance of the total output stage is subtracted from this number, we are left with the net allowed case-to-ambient thermal resistance ($R_{\theta CA}$) of 0.843°C/W. This value includes any thermal resistance due to the insulating washers that must be used to prevent the transistors from making electrical contact with the heat sink (often as much as 0.3°C/W per insulator). Thus in reality, some allowance for the interface materials must be made in the choice of the final extrusion which will provide heatsinking for the power transistors. In the example here, a large finned heatsink with a sink-to-ambient thermal resistance ($R_{\theta SA}$) of around 0.69°C/W is required. Of course, had two pairs of transistors been used in the output stage, the net $R_{\theta JC}$ would have been lower by a factor of two and a smaller extrusion could have been used for the heatsink. Thus there is a limited trade-off that can be made between the number of transistors and the size of the output stage heatsink, for a given power supply rail voltage and load impedance.

MEASURED PERFORMANCE

Table I provides a synopsis of the overall performance of the current feedback power amplifier using the new complementary IGBT output devices. Although this design does not achieve astoundingly low distortion levels typical of more complex topologies that employ linearization schemes in the output stage, the measurements made show that the THD and IMD generated by this circuit are still respectably low. Figure 8 shows that the overall harmonic distortion at 50 W output into an 8 Ω load is a minimal 0.001% at 1 kHz, rising to just under 0.009% at 20 kHz. This is a particularly good result considering that only one pair of output transistors has been used. Also, no low-pass LR isolation network has been used in series with the output that would tend to

attenuate the high frequency harmonics. This would artificially improve the amplifier performance in the vicinity of 20 kHz, and was deliberately excluded. SMPTE intermodulation distortion for 60 Hz and 7 kHz mixed 4:1 is plotted in Figure 9 as a function of the rms input level and, as the curve indicates, it is extremely low being just 0.0004% at 41.7 W into 8 Ω (0.92 V rms input). The absence of any significant upward slope in the curve of Figure 9, except where the amplifier is entering its overload region at about 0.95 V rms input, indicates a lack of thermal modulation effects on the 750 Ω feedback resistor.

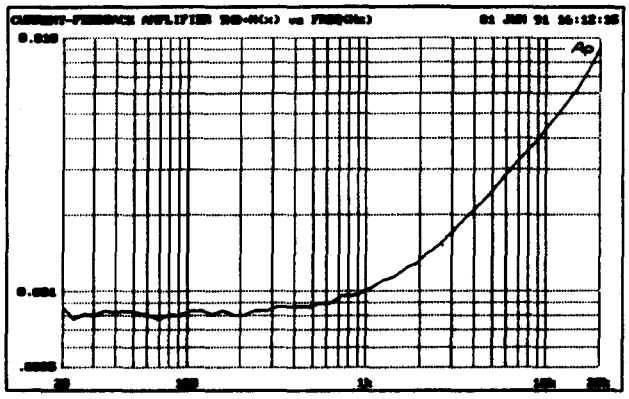


Figure 8. Amplifier THD Is Below 0.009% Throughout the Audio Band When Delivering 50 W to An 8 Ω Load.

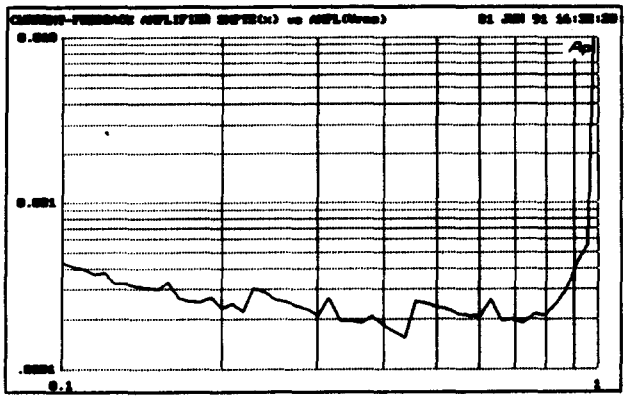


Figure 9. SMPTE Intermodulation Distortion (60 Hz/7 kHz 4:1, 40 W into 8 Ω) Is Exceptionally Low, Reaching Almost 0.0002% Before Rising as the Amplifier Enters its Overload Region.

Table 1. Summary of Amplifier Performance (V_{SUPPLY} = ±40 V, Current Limited to 2.5 A Average Per Rail, R_L = 8 Ω)

Sine Wave Power Output (Voltage Limited)	70 W
Total Harmonic Distortion at 1 kHz	0.001% at 50 W
Total Harmonic Distortion at 20 kHz (Depends Strongly on Idling Current Level in Output Stage)	0.009% at 50 W
SMPTE Intermodulation Distortion	0.0004% at 41.7 W
Dynamic Intermodulation Distortion (DIM-100)	0.0012% at 50 W
Frequency Response (−3 dB)	DC to 1 MHz
Slew Rate	>200 V/μs
Rise Time (Input Filter in Circuit)	400 ns
Total Quiescent Supply Current	130–150 mA

Static distortion measurements aside, what does put the current feedback topology into a class of its own is the dynamic performance. High slew rate is always critical in any large signal amplifier design, but proper waveform control during the reproduction of a square wave is just as important. Because of the nature of the gain stage arrangement in this amplifier, slew rate limiting occurs at a very large rate of change (typically 250 V/μs). Most normal program material is unlikely ever to cause slew limiting in this amplifier, even with large output swings. Consequently, the value measured for the DIM-100 dynamic intermodulation distortion test is a very low 0.0012% at 50 W output into 8 Ω, as shown in Figure 10.

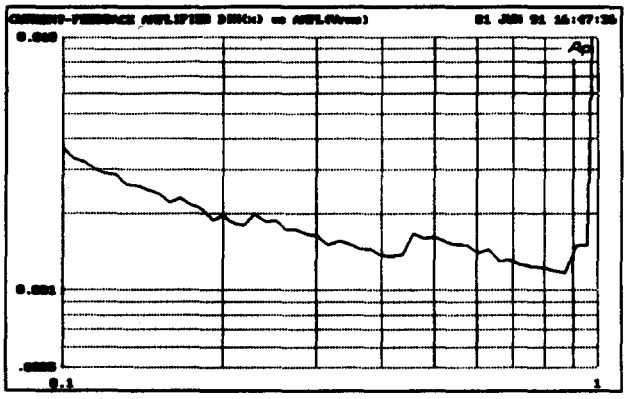


Figure 10. Low DIM-100 Transient Intermodulation Distortion (3.15 kHz/15 kHz 4:1, 50 W into 8 Ω) Results from the Clean Transient Response.

This is the lowest value of DIM-100 distortion that the author has ever seen reported for a solid-state power amplifier. In numerous listening tests, the "fast" sound of this amplifier and its tight LF performance have been commented upon. The large signal step response of the amplifier into an 8 Ω load at 100 kHz is shown in Figure 11, and the no load response with an 80 V p–p square-wave at the output is shown in Figure 12. Either photograph reveals that the amplifier is inherently stable and exhibits no trace of overshoot on fast edges.

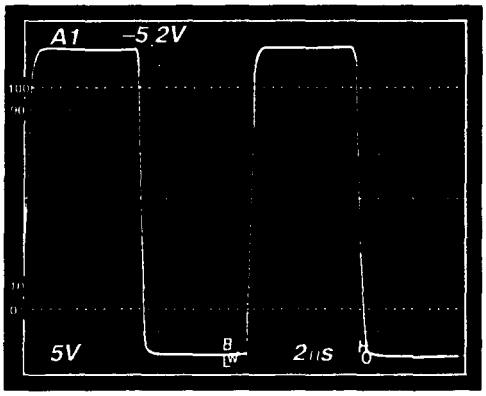


Figure 11. The Amplifier Exhibits Minimal Overshoot When Driving a High Frequency Square Wave into an 8 Ω Load.

Finally the frequency response, as shown in Figure 13, does indeed verify the somewhat overbearing calculations done earlier and proves that the closed-loop bandwidth extends all the way out to 1 MHz. Such a wide frequency response is definitely overkill for any audio power amplifier (200 kHz–300 kHz is probably more than adequate), but it does show what is achievable with a modern design.

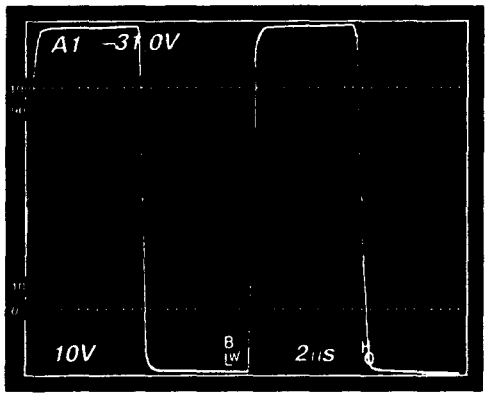


Figure 12. A Large Signal Square Wave at 100 kHz Shows that the IGBT Output Stage Is Inherently Stable Even Without a Load.

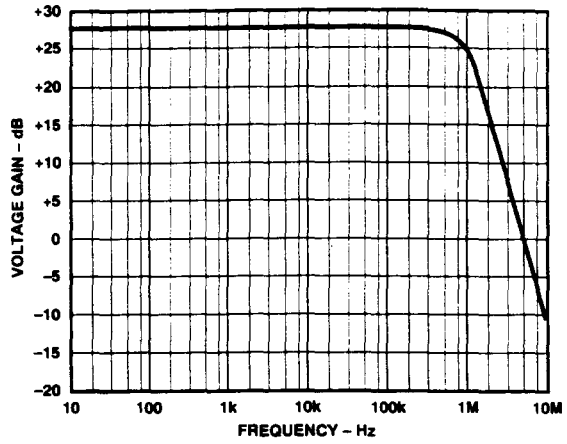


Figure 13. The Small-Signal Frequency Response Does Indeed Extend All the Way Out to 1 MHz, as Predicted by the Calculations.

CONCLUSION

Once in a while a new design comes along that offers a different way of doing an old job. The amplifier that has been presented here offers an evolutionary approach to the task of driving a loudspeaker. When proper attention is paid to all the details (and some of them are nontrivial indeed), current feedback amplifiers can offer superior sonic performance to all known topologies.

REFERENCES

[1]Mark Alexander, "A Current Feedback Audio Power Amplifier," 88th Convention of the Audio Eng. Soc., reprint #2902, March 1990.

[2]Edward M. Cherry, "A New Distortion Mechanism in Class B Amplifiers," Journal of the Audio Eng. Soc., Vol 29, No. 5, pp. 327-32 8, May 1981.

APPENDIX A: FREQUENCY RESPONSE OF CURRENT FEEDBACK AMPLIFIERS

To derive the input-to-output transfer function of a current feedback amplifier, the representative model shown in Figure 14 must be analyzed. Instead of a differential input stage, this topology utilizes a unity gain input buffer, driving a low impedance current summing node, which forces the inverting terminal to be at the same potential as the noninverting input. A nonzero input buffer output resistance, R_{INV}, is shown in series with the inverting terminal and must be included in the analysis of closed-loop gain versus frequency. Neglecting this resistance is a common oversight in simplified analyses, and leads to a transfer function that will not show any bandwidth variation with gain at all. Feedback is applied from the main amplifier output back to the inverting terminal through the current summing network that comprise of R_1 and R_2.

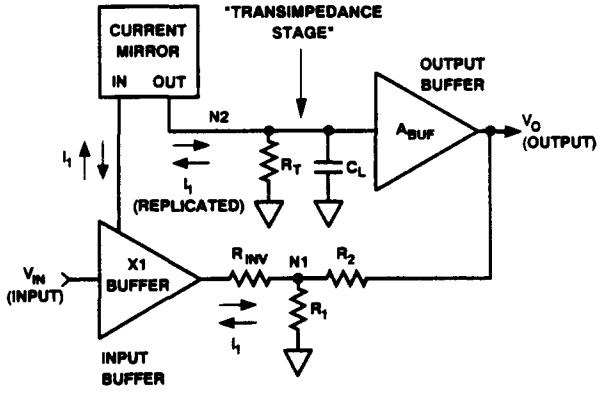


Figure 14.

The action of the input buffer is to force a finite current to flow through R_1 that must be balanced by an almost exactly equal but opposite current in R_2. Any difference between these two currents is an error current that flows into or out of the low impedance inverting terminal. This error current (as opposed to an error voltage in a conventional operational amplifier) is then mirrored and fed into a transimpedance stage, consisting of R_T and Cc, where current-to-voltage conversion takes place. The voltage generated here is buffered by another unity gain stage and is fed to the main amplifier output. Because the value of the small signal transresistance, R_T, is very high (normally several megohms) only minute error currents are needed to change the voltage at node 2 by several volts. Consequently, the amount of current that must flow into or out of the inverting terminal under steady state conditions is extremely small. The feedback network, even though it consists of fairly low value resistors, therefore presents a very light effective load on the output of the input buffer. To derive a transfer function for this amplifier, nodal equations must be written for nodes 1 and 2, and then combined in an appropriate way to obtain the final result:

$$\frac{V_O}{V_{IN}} = \frac{1+\frac{R_2}{R_1}}{1+\frac{R_2+\left(1+\frac{R_2}{R_1}\right)R_{INV}}{R_T A_{BUF}}+s\frac{\left(R_2+\left(1+\frac{R_2}{R_1}\right)R_{INV}\right)C_C}{A_{BUF}}} \quad (7)$$

This relationship is actually very similar to that of a voltage feedback amplifier, and it can be seen that the dc closed-loop gain is nearly equal to $1 + R_2/R_1$ (assuming that the product $R_T A_{BUF}$ is also reasonably large). The low frequency gain term is something with which most users of IC op amps should already be familiar. At a first glance the frequency dependent term might seem to be quite similar to that of a voltage feedback amplifier, but it is in fact very different. This can be seen more easily if the expression for the closed-loop pole frequency is written down:

$$f_{POLE} \cong \frac{A_{BUF}}{2\pi\left(R_2+\left(1+\frac{R_2}{R_1}\right)R_{INV}\right)C_C} \quad (8)$$

Interestingly, this result shows that the pole frequency now depends predominantly on the value of feedback resistor R_2 and the input buffer output resistance R_{INV} multiplied by the closed-loop gain. Normally the value of R_{INV} is made as low as possible to minimize the change in pole frequency with gain, and is typically less than one tenth that of the minimum recommended feedback resistor value. At high gains, as mentioned before, the closed-loop bandwidth starts to become inversely proportional to the gain because the term in the denominator of Equation (8) due to R_{INV} starts to become dominant. The gain bandwidth product is thus:

$$GBW = \frac{A_{BUF}}{2\pi R_{INV} C_C} \quad (9)$$

The gain of the output buffer, A_{BUF}, also plays its part in determining the closed-loop pole frequency. As the main amplifier output is loaded, this gain drops well below unity, and causes a reduction in closed-loop bandwidth as dictated by Equation (8). This actually tends to make the amplifier more stable since the high frequency nondominant poles contribute less additional phase shift at the lower closed-loop −3 dB point. In fact, many commercial current feedback amplifiers show significant gain peaking with light loads, and don't begin to behave acceptably until loaded fairly heavily. Another thing to remember is that the minimum recommended

value for feedback resistor R_2 must be strictly adhered because too low a value will result in an excessively high closed-loop pole frequency. This can result in severe gain peaking due to the higher order poles becoming more dominant, and is especially a problem at low gains when the multiplicative effect of R_{INV} on the closed-loop pole time constant is minimal.

During early development of the current feedback power amplifier it was noticed that instability appeared on the edges of square waves, using the ground referenced compensation scheme. Some experimentation revealed that connecting the compensation capacitors to the feedback summing node made the instability disappear. An analysis of the amplifier response using this new arrangement was undertaken, since something must have changed to make it more stable. Indeed, when the compensation capacitors are returned to the feedback summing node instead of ground, the transfer function of the circuit changes quite significantly. This modified compensation arrangement also allows one to get by with smaller capacitors than before, but without compromising closed-loop stability. To see this, the current feedback model must be analyzed again but this time the compensation capacitor C_C is returned to the summing node instead of ground:

$$\frac{V_O}{V_{IN}} = \frac{\left(1 + \frac{R_2}{R_1}\right)\left(1 + s\left(\frac{2R_1R_2C_C}{R_1 + R_2}\right)\right)}{1 + \frac{R_2 + \left(1 + \frac{R_2}{R_1}\right)R_{INV}}{R_TA_{BUF}} + s\left(\frac{2R_2C_C + \left(1 + \frac{R_2}{R_1} + \frac{R_2}{R_T}\right)R_{INV}C_C}{A_{BUF}} - R_{INV}C_C\right)} \quad (10)$$

The major difference between Equations (7) and (10) is the appearance of a zero in the numerator determined by the parallel combination of R_1 and R_2, and some additional terms in the denominator. The zero tends to partially cancel the second pole of the amplifier due to the IGBT output stage, resulting in greatly improved stability. Probably the most interesting thing to notice about Equation (10) however, is that the R_2C_C time constant is now multiplied by a factor of two instead of unity as before. Since it is this time constant that predominantly determines the closed-loop pole frequency, the original compensation capacitor value can thus be scaled down by a factor of one half.

APPENDIX B: AMPLIFIER COMPONENT LIST FOR A SINGLE CHANNEL

	Quantity	Designator
Integrated Circuits		
SSM-2131P BiFET Audio Op Amp	1	A_1
OP-97FP Precision DC Op Amp	1	A_2
TL431CP Programmable Shunt Regulator	1	D_7
Transistors		
2N3904 NPN, 40 V (4 Are Used as Zener diodes)	7	Q_5, Q_7, Q_{12}, Q_{14}–Q_{17}
2N3906 PNP, 40 V	2	Q_3, Q_{13}
2N5401 PNP, 150 V (or 2SC2682 from NEC)	3	Q_2, Q_4, Q_9
2N5551 NPN, 160 V	3	Q_1, Q_6, Q_8
MPS-U10 NPN, 300 V[1]	1	Q_{10}
MPS-U60 PNP, 300 V[2]	1	Q_{11}
GT20D101-Y N-CHAN IGBT 250 V, 20 A (Toshiba)	1	Q_{18}
GT20D201-Y P-CHAN IGBT 250 V, 20 A (Toshiba)	1	Q_{19}
Diodes		
1N914 100 V, 100 mA Small Signal Diode	9	D_1, D_2, D_5, D_6, D_8, D_{11}, D_{12}, D_{13}, D_{14}
1N5242B 12 V, 500 mW Zener Diode	2	D_9, D_{10}
1N4938 200 V, 100 mA Low t_{RR} Diode	2	D_3, D_4
MR822 200 V, 5 A Low t_{RR} Rectifier	2	D_{15}, D_{16}
Resistors		
(All Values Are in Ohms, and Are 1/4W 1% Metal Film Unless Otherwise Specified)		
0.05 Ω, 3 W, 5% Noninductive (Shallcross LO-3 Series)	2	R_{24}, R_{25}
10.0	2	R_{19}, R_{20}
16.5	1	R_7
33.2	1	R_6
100 (2 Are Used as Gate Resistors for the IGBTs)	7	R_3, R_{13}–R_{16}, R_{23}, R_{26}
249	1	R_{22}
499	1	R_{10}
750, 2-5 W, 1% Noninductive Metal Film	1	R_8
4.99 k	1	R_{12}
10.0 k	1	R_{21}
11.5 k	1	R_{11}
16.9 k	1	R_{17}
24.9 k	1	R_{18}
100 k	1	R_4
1.00 M	2	R_5, R_9
R_{BIAS} (49.9 k with ±65 V Power Rails)	2	R_1, R_2
50 kΩ Multiturn Trimpot (Helitrim 68WR503 or Equivalent)	1	VR_1
Capacitors		
47 pF 5% Silvered Mica (or Ceramic) 200 V	2	C_6, C_7
750 pF 5% Silvered Mica (or Ceramic) 200 V	1	C_3
0.1 μF 10% Ceramic or Mylar 63 V	4	C_4, C_5, C_8, C_{10}
1 μF 10% Ceramic 100 V	1	C_{11}
2 μF 10% Polyfilm 100 V (Electrocube 230B1B205K)	2	C_{12}, C_{13}
10 μF 10% Tantalum Electrolytic 25 V	3	C_1, C_2, C_9
2 to 10 μF 10% Polyfilm 100 V	2	C_{16}, C_{17}
220 or 330μF 10% Aluminum Electrolytic 100 V	2	C_{14}, C_{15}
Miscellaneous:		
Form-C Reed Relay (Coto 2211-12-300)	1	K_1
Thermalloy 6100B Heatsink for the Driver Transistors	2	
Extra Large Finned Heatsink for the IGBT Output Stage	1	
Insulating Pads for the IGBTs	2	
5-Pin Molex Header 0.156 Inch Pin Spacing	1	
7-Pin Molex Header 0.156 Inch Pin Spacing	1	
3-Pin Molex Header 0.100 Inch Pin Spacing	1	
Right Angle RCA Jack	1	
Amplifier evaluation PC Board[3]	1	

[1]First choice substitution is NEC 2SC2682; second choice Toshiba 2SC2238B. Note correct pinouts.
[2]First choice substitution is NEC 2SA1142; second choice Toshiba 2SA968B. Note correct pinouts.
[3]Available to qualified OEMs. Contact local ADI sales office for details.